Module 14: **CMOS cell layout 2**

Learning objectives:

Study of the following topics –

Stick diagrams

Cell partitioning

Floor planning

This module is the second of two dealing with the layout of digital circuits in CMOS technology. It mainly deals with the topic of stick diagrams. This is an important aid in laying out CMOS circuits. The rules for drawing stick diagrams are discussed. Stick diagrams for a CMOS inverter and for a simple combinational logic circuit are described. CMOS cell partitioning and floor planning are the last topics discussed in this module.

First go through the Powerpoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

There are no reading assignments for this module.

Questions

Q1. Draw stick diagrams for a 2-input NAND gate, a 2-input NOR gate, a 2-input AND gate and a 2-input OR gate.